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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/697,197	10/30/2003	Ernest S. Cohen	MSFT-2819/305829.1	2215

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EXAMINER
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YU, JAE UN

ART UNIT	PAPER NUMBER
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2185

DATE MAILED: 12/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/697,197	COHEN, ERNEST S.	
	<b>Examiner</b>	<b>Art Unit</b>	
	Jae U. Yu	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 30 October 2003.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-24 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-24 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 30 October 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>3/10/2004</u> . | 6) <input type="checkbox"/> Other: _____  |

The instant application having Application No. 10/697,197 has a total of 24 claims pending in the application, there are 4 independent claims and 20 dependent claims, all of which are ready for examination by the examiner.

***Oath/Declaration***

The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in 37 C.F.R. 1.63.

***Drawings***

The applicant's drawings submitted on 10/30/2003 are acceptable for examination purposes.

***Information Disclosure Statement***

As required by M.P.E.P. 609(C), the applicant's submission of the Information Disclosure Statement dated 3/10/2004 is acknowledged by the examiner and the cited references have been considered in the examination of the claims now pending. As required by M.P.E.P. 609C(2), a copy of the PTOL-1449 initialed and dated by the examiner is attached to the instant office action.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 1-24 are rejected under 35 U.S.C. 102(b) as being anticipated by Harvey et al. (US 6,233,668 B1).
2. **Claim 1** recites, "For at least one of the plurality of page tables, creating a first shadow page table based on said one of the plurality of page tables". **In column 4, at lines 1-3, Harvey et al. recites, "The use of a page table that is a composite of a plurality of constituent self-mapping page-tables that coincide in virtual-address."** The "self-mapping" page-tables correspond to the "shadow page table" from the claim. "At least one entry in said first shadow page table links to a different data page than that entry's corresponding link in said first one of the plurality of page tables". **In column 4, at lines 11-15, Harvey et al. recites, "Each substructure is a constituent page table that coincides in virtual-address space with other constituent page tables but is materialized in different physical-address locations, whose contents are not in general identical to those of other constituents."** It discloses the pages tables that have the same virtual address but link to different physical addresses. The

“substructure” corresponds to the “shadow page table” from the claim, and the “physical-address locations” corresponds to the “data page” from the claim.

“Said first shadow page table contains one or more read-only links whose corresponding links in said first one of the plurality of pages tables are read/write”. In column 17, at lines 2-6, Harvey et al. recites, **“Since this flag is encountered in the translation buffer during a translation that would yield a page frame containing a version of the top level subtable, the write operation does not occur.”** When the flag is set, the operation is write-protected which means it is “read-only”. The “translation buffer” contains the “shadow page table” from the claim, and it is “write-protected” (“read-only”) link.

“Creating a shadow page directory based on the page directory, the page directory comprising a link to said one of the plurality of page tables, said shadow page directory comprising a link to said shadow page table instead of the link to said one of said plurality of page tables”. In column 7, at lines 1-2, Harvey et al. recites, **“FIG. 3’s reference numeral 96 represents the self-mapping nature of that entry”**, which means that the “top-level index (76)” creates a “shadow page” of itself. In column 4, at lines 11-15, Harvey et al. recites, **“Each substructure is a constituent page table that coincides in virtual-address space with other constituent page tables but is materialized in different physical-address locations, whose contents are not in general identical to those of other constituents”**, which means that the “self-mapped pages” at the same virtual-memory location link to different addresses than each other.

3. **Claim 2** recites, "Access to said memory based on said address translation map applied to said virtual address results in violation of said policy, and wherein access to said memory based on said shadow page directory and said first shadow page table being applied to said virtual address does not result in violation of said policy." In **column 15, at lines 13-16, Harvey et al. recites, "This exception handler has been arranged in the illustrated embodiment to determine whether a true access violation has actually occurred"**, which corresponds to the "policy" from the claim. In **column 15, at lines 26-31, Harvey et al. recites, "The handler compares the faulting reference with the shared/physical boundary to determine which of the two physical page frames identified by FIG. 3's registers 38 and 122 is the one that properly contains the page translation for that reference, and it fetches the proper entry by physical addressing."** The "faulting reference" corresponds to the "virtual address results in violation" from the claim, and "fetching the proper entry by physical addressing" corresponds to the "virtual address does not result in violation" from the claim.

4. **Claim 3** recites, "Each of the data pages is stored at a particular frame of a memory, wherein said page directory is stored at a first frame." In **figure 3, Harvey et al. shows the "data page frames" which corresponds to the "data pages" from the claim, and the "top-level index" which corresponds to the "first frame" from the claim.** "Maintaining a copy of said page directory at a second frame different from said first frame." In **column 9, at lines 25-28, Harvey et al. recites, "The subtables located at**

**some virtual-memory locations have different versions for different processes, and each is therefore materialized in different physical memory**", which means that the copies of the subtables are maintained in the different physical memory locations which corresponds to the "second frame different from said first frame" from the claim. "Storing the shadow page directory at said first frame." **In figure 3**, the self-mapped TLST (96) is stored at the same page frame.

5. **Claim 4** recites, "Page directory comprises a link to a first-sized page, said first-sized page comprising a plurality of second-sized pages." **In column 6, at lines 31 to 33, Harvey et al. recites, "An advantage of a multi-level page table is that it can manage large numbers of pages but requires little table space when the number of pages is small"**, which means that referring to **figure 3**, the "top-level index (76)" (corresponding to the "page directory" from the claim) links to the multiple "middle-level indexes (78, 80)" (corresponding to the "second-sized pages" from the claim). "Creating a second shadow page table that comprises links to a said plurality of second sized pages, wherein said shadow page directory comprises a link to said second shadow page table." **In figure 3**, the "middle-level index" (corresponding to the "second shadow page table" from the claim) links to the "bottom-level index" (corresponding to the "second sized pages" from the claim), and the "top-level index" (corresponding to the "shadow page directory" from the claim) links to the "middle-level index" (corresponding to the "second shadow page table").

6. **Claim 5** recites, “A memory comprising a plurality of individually-addressable components that can be read and written, each of the individually-addressable components having a physical address.” **In column 4, at lines 11-13, Harvey et al. recites, “A constituent page table that coincides in virtual-address space with other constituent page tables but is materialized in different physical-address locations.”** The “physical-address locations” corresponds to the “individually-addressable components having a physical address” from the claim.

“A mapping between virtual addresses and the physical addresses.” **In column 5, at lines 30-33, Harvey et al. recites, “A page table, whose entries indicate the physical locations of “page frames” that contain respective virtual memory “pages”.”**

“Memory manager translating said virtual address into the physical address of said first one of the individually-accessible components based on data that comprises a shadow representation of said address translation structure.” **In figure 1, the “MMU” with the “translation buffer” corresponds to the “memory manager” from the claim. In column 9, at lines 25-28, Harvey et al. recites, “The subtables located at some virtual-memory locations have different versions for different processes, and each is therefore materialized in different physical memory.”** There are multiple versions for the “subtables” (corresponding to the “shadow representation” from the claim), and they are “materialized” (“translated”) to the “physical memory”.



7. **Claim 6** recites, “A plurality of page tables that contain links to said plurality of pages.” In **figure 3**, the “byte-within page (60)” corresponds to the “plurality of pages” from the claim, and the “bottom-level index (94)” corresponds to the “plurality of page tables” from the claim.

“A page directory that contains links to said plurality of page tables, and wherein said shadow representation of said address translation structure differs from said address translation structure with respect to at least one link.” In **figure 3**, Harvey et al. shows the “top-level index (84)” (corresponding to the “page directory” from the claim) linking to the lower-level indexes (corresponding to the “page tables” from the claim). In **column 4, at lines 11-14, Harvey et al. recites, “A constituent page table that coincides in virtual-address space with other constituent page tables but is materialized in different physical-address locations”**. The “constituent page table that coincides in virtual-address space with other constituent page tables” corresponds to the “shadow representation” from the claim. It links to the different “physical-address location”.

8. **Claim 7** recites, “At least one link in said shadow representation differs from a corresponding link in said address translation structure with respect to at least one attribute”. In **column 4, at lines 14-15, Harvey et al. recites, “Whose contents are not in general identical to those of other constituents.”** The “whose contents” refer to the contents in the “different physical-address location”, and they correspond to the “attribute” from the claim.

9. **Claim 8** recites, "Each of the links in the page directory and page tables identifying one of the pages based on the physical location descriptor." **In column 5, at lines 30-33, Harvey et al. recites, "Each process is given a page table, whose entries indicate the physical locations of "page frames" that contain respective virtual memory "pages".** The page table corresponds to the "descriptor" from the claim, and it links (identifies) virtual locations to physical locations.

10. **Claim 9** recites, "Alternative version is stored at a page having a different physical location descriptor from the page on which the alternative version is based." **In column 9, at lines 25-28, Harvey et al. recites, "Subtables located at some virtual-memory locations have different versions for different processes, and each is therefore materialized in different physical memory."** The "different versions for different processes" correspond to the "alternative version" from the claims, and they are materialized in different physical memory.

11. **Claim 10** recites, "A memory access control manager that creates the shadow representation based on the address translation structure and ensures that the shadow representation, if used to access the memory based on virtual addresses, does not result in violation of the policy." **In column 15, at lines 13-16, Harvey et al. recites, "This exception handler has been arranged in the illustrated embodiment to determine whether a true access violation has actually occurred",** which corresponds to the "policy" from the claim. **In column 15, at lines 26-31, Harvey et al.**

**recites, “The handler compares the faulting reference with the shared/physical boundary to determine which of the two physical page frames identified by FIG. 3’s registers 38 and 122 is the one that properly contains the page translation for that reference, and it fetches the proper entry by physical addressing.”** The virtual address linking to the “proper” physical address is fetched so it would not violate the policy.

12. **Claim 11** recites, “The policy defines a portion of the memory as inaccessible, and wherein the memory access control manager ensures that the shadow representation does not expose a virtual address for said portion of the memory.” In column 15, at lines 12-16, Harvey et al. recites, “Invalid-access-exception handler, this exception handler has been arranged in the illustrated embodiment to determine whether a true access violation has actually occurred”, which corresponds to the “policy” from the claim. In column 15, at lines 26-31, Harvey et al. recites, “The handler compares the faulting reference with the shared/physical boundary to determine which of the two physical page frames identified by FIG. 3’s registers 38 and 122 is the one that properly contains the page translation for that reference, and it fetches the proper entry by physical addressing.” The virtual address linking to the “proper” physical address is fetched so it would not violate the policy.

13. **Claim 12** recites, "The policy defines a portion of the memory as being readable but not writeable, and wherein the memory access control manager ensures that the shadow representation contains one of more attributes that mark the portion of memory as being read-only." In column 17, at lines 2-6, Harvey et al. recites, **"Since this flag is encountered in the translation buffer during a translation that would yield a page frame containing a version of the top level subtable, the write operation does not occur."** When the flag (determines whether the memory is writable or not) is set, the operation is write-protected which means it is "read-only". The "translation buffer" contains the "shadow representation" from the claim, and it is "write-protected" ("read-only") link.

14. **Claim 13** recites, "The shadow representation contains one or more attributes that mark as read-only those portions of the memory that store at least one of: (1) the address translation structure; and (2) the shadow representation." In column 17, at lines 1, Harvey et al. recites, **"The illustrated embodiment write protects the top-level subtable."** The "top-level subtable" (76 from figure 3) corresponds to the "address translation structure" from the claim. Also, the self-mapped "top-level subtable (96) corresponds to the "shadow representation" from the claim.

15. **Claim 14** recites, "Receiving an request to read or write a unit of a memory, said request identifying said unit of said memory based on a virtual address." In column 5, at lines 30-33, Harvey et al. recites, **"Each process is given a page table, whose**

**entries indicate the physical location of “page frames” that contain respective virtual memory “pages”.** The “physical location” corresponds to the “memory” from the claim, and it is mapped (identified) by the virtual address.

“Accessing said unit of memory based on a representation of a map that defines a relationship between virtual addresses and physical addresses.” **In column 5, at lines 30-33, Harvey et al. recites, “Each process is given a page table, whose entries indicate the physical location of “page frames” that contain respective virtual memory “pages”.**”

“At least one shadow page that is based on a first one of said one or more pages.” **In column 4, at lines 1-3, Harvey et al. recites, “The use of a page table that is a composite of a plurality of constituent self-mapping page-tables that coincide in virtual-address.”** The “self-mapping page-tables” corresponds to the “shadow page” from the claim.

“Said map including at least one aspect which, if used to access said memory based on said virtual address, would result in violation of a memory access policy, said shadow page differing from said first one of said one or more pages in a manner such that use of said representation of said map to access said memory based on said virtual address does not violate said memory access policy. Performing the read or write specified in said access request.” **In column 15, at lines 13-16, Harvey et al. recites, “This exception handler has been arranged in the illustrated embodiment to determine whether a true access violation has actually occurred”,** which corresponds to the “policy” from the claim. **In column 15, at lines 26-31, Harvey et al. recites, “The**

**handler compares the faulting reference with the shared/physical boundary to determine which of the two physical page frames identified by FIG. 3's registers 38 and 122 is the one that properly contains the page translation for that reference, and it fetches the proper entry by physical addressing.** The "faulting reference" corresponds to the "virtual address results in violation" from the claim, and "fetching the proper entry by physical addressing" corresponds to the "virtual address does not result in violation" from the claim.

16. **Claim 15** recites, "Said memory access policy defines a portion of said memory as being inaccessible, wherein said map exposes writeable links to portions of said memory that define virtual address mappings, and wherein said representation of said map does not expose writeable links to portions of said memory that define virtual address mappings." In column 15, at lines 12-16, Harvey et al. recites, "Invalid-access-exception handler, this exception handler has been arranged in the illustrated embodiment to determine whether a true access violation has actually occurred", which corresponds to the "policy" from the claim. In column 17, at lines 2-6, Harvey et al. recites, "Since this flag is encountered in the translation buffer during a translation that would yield a page frame containing a version of the top level subtable, the write operation does not occur." When the flag (determines whether the memory is writable or not) is set, the operation is write-protected which means it is "read-only". The "translation buffer" contains the "shadow representation" from the claim, and it is "write-protected" ("does not expose writeable link").

17. **Claim 16** recites, “A plurality of tables that contain links to a set of said one or more pages. A directory that contains links to said plurality of tables.” **Figure 3** shows the plurality of tables that links to the lower-level pages, and “TLST” (76) corresponds to the “directory” from the claim.

“Said at least one shadow page comprising a shadow directory that differs from said directory in at least the respect that at least one link in the shadow directory points to a shadow page table instead of to one of said plurality of tables.” **In column 9, at lines 25-27, Harvey et al. recites, “The subtables located at some virtual-memory locations have different versions for different processes.”** The “subtables” corresponds to the “shadow page table” from the claim, and “TLST” points to it as disclosed in **figure 3**.

18. **Claim 17** recites, “First link is a read/write link in said one of said tables, and wherein said shadow page differs from said one of said tables in that said shadow page’s representation said first link is marked read-only.” **In column 17, at lines 2-6, Harvey et al. recites, “Since this flag is encountered in the translation buffer during a translation that would yield a page frame containing a version of the top level subtable, the write operation does not occur.”** When the flag is set, the operation is write-protected which means it is “read-only”. The “translation buffer” contains the “shadow page” from the claim, and it is “write-protected” (“read-only”) link.

19. **Claim 18** recites, "Said shadow pages differs from said directory in that said shadow page contains a link to a table instead of a link to said first-sized page, wherein said table contains links to second-sized pages." **In figure 3**, the "middle-level index" (corresponding to the "shadow page" from the claim) links to the "bottom-level index" (corresponding to the "second-sized pages" from the claim), and the "top-level index" (corresponding to the "directory" from the claim) links to the "middle-level index" (corresponding to the "first-sized page").

20. **Claim 19** recites, "A shadow page table that is based on a first one of the plurality of page tables. A shadow page directory that is based on the page directory." **In column 4, at lines 1-5, Harvey et al. recites, "The use of a page table that is a composite of a plurality of constituent self-mapping page-tables that coincide in virtual-address space."** The "self-mapping page-tables" (corresponding to the "shadow page table/directory" from the claim) are based on the "page table" (corresponding to the "page tables/directory" from the claim).

"Said shadow page table comprising a second entry that corresponds to the first entry, said second entry containing a link to said shadow page table instead of a link to said first one of the plurality of page tables." **In column 4, at lines 11-15, Harvey et al. recites, "Each substructure is a constituent page table that coincides in virtual-address space with other constituent page tables but is materialized in different physical-address locations, whose contents are not in general identical to those of other constituents."** The "constituent page table that coincides in virtual address"



corresponds to the “second entry that corresponds to the first entry” from the claim. The “different physical-address locations” corresponds to the “link to said shadow page table” from the claim.

21. **Claim 20** recites, “The shadow page directory differs from the page directory in the respect that a link in the page directory contains an identifier of said first frame and the corresponding link in the shadow page directory contains an identifier of said second frame.” In column 4, at lines 11-15, Harvey et al. recites, “Each substructure is a constituent page table that coincides in virtual-address space with other constituent page tables but is materialized in different physical-address locations, whose contents are not in general identical to those of other constituents.” The “constituent page table” corresponds to the “shadow page directory” from the claim because they have the same virtual addresses. They link to different “frames” as disclosed in the claim because they are materialized in “different physical locations” to each other.

22. **Claim 21** recites, “Said shadow page table contains a link to a representation based on said first one of the pages instead of the link to the first one of the pages, said representation based on said first one of the pages being stored at a frame different from said first one of the pages.” In column 9, at lines 25-28, Harvey et al. recites, “The subtables located at some virtual-memory locations have different versions for different processes, and each is therefore materialized in different physical

**memory**", which means that the copies of the subtables are maintained in the different physical memory locations which corresponds to the "different frame" from the claim, and the "subtables" corresponds to the "shadow page table" from the claim.

23. **Claim 22** recites, "First one of the plurality of pages stores either the page directory or said first one of the plurality of page tables." The "plurality of pages" corresponds to the "TLST and MLST page frames" in **figure 3**. The "page directory" corresponds to the "top-level index" in **figure 3**, and the "page tables" corresponds to the "middle-level index" in **figure 3**.

24. **Claim 23** recites, "First one of the plurality of page tables contains a link that specifies said first one of the plurality of pages as being readable and writeable, and wherein the corresponding link in said shadow page table specifies said first one of the plurality of pages as being only readable." **In column 17, at lines 2-6, Harvey et al. recites, "Since this flag is encountered in the translation buffer during a translation that would yield a page frame containing a version of the top level subtable, the write operation does not occur."** When the flag is set, the operation is write-protected which means it is "read-only". The "translation buffer" contains the "shadow page table" from the claim, and it is "write-protected" ("read-only") link.

25. **Claim 24** recites, "The shadow page directory and shadow page table contain data such that accessing the memory through said shadow page directory and said

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shadow page table on said virtual address does not result in violation of said memory access policy.” In column 15, at lines 13-16, Harvey et al. recites, “**This exception handler has been arranged in the illustrated embodiment to determine whether a true access violation has actually occurred**”, which corresponds to the “policy” from the claim. In column 15, at lines 26-31, Harvey et al. recites, “**The handler compares the faulting reference with the shared/physical boundary to determine which of the two physical page frames identified by FIG. 3’s registers 38 and 122 is the one that properly contains the page translation for that reference, and it fetches the proper entry by physical addressing.**” The “faulting reference” corresponds to the “virtual address results in violation” from the claim, and “fetching the proper entry by physical addressing” corresponds to the “virtual address does not result in violation” from the claim.

### ***Relevant Art Cited by the Examiner***

The following prior art made of record and not relied upon is cited to establish the level of skill in the applicant’s art and those arts considered reasonably pertinent to applicant’s disclosure. See MPEP 707.05(C).

The following reference teaches a **self-mapping virtual memory** that corresponds to multiple physical memory locations.

### **Non-Patent Literature**

Harvey et al., Extending Open VMS for 64-Bit

### **Figures**

3 and 4

Addressable Virtual Memory, *Digital Technical Journal*, vol. 8, No. 2 (1996).

### ***Conclusion***

#### **1. Claims Rejected in the Application**

Per the instant office action, claims 1-24 have received a first action on the merits and are subject of a first action non-final.

#### **2. Directions of Future Correspondences**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jae U. Yu whose telephone number is 571-272-1133. The examiner can normally be reached on M-F 9AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald A. Sparks can be reached on 571-272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Application/Control Number: 10/697,197

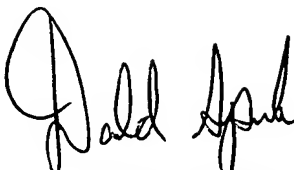
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December 19, 2005

Jae Un Yu  
Patent Examiner  
Art Unit 2185

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DONALD SPARKS  
SUPERVISORY PATENT EXAMINER